REMARKS/ARGUMENTS

In the Office Action mailed June 10, 2008, claims 1-12 were rejected. In response, Applicants hereby request reconsideration of the application in view of the below-provided remarks. No claims are amended or canceled.

For reference, new claims 13-20 are added. Each of these claims recites further limitations of the host controller, including a memory mapped input/output, a memory management unit, a slave DMA controller, registers, a logic unit, an internal bus, and a connection for control and interrupt signals. These claims are supported, for example, by the subject matter described at page 3, lines 6-15, of the specification.

Claim Rejections under 35 U.S.C. 103

Claims 1-12 were rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (US. Pat. Pub. No. 2002/0116565, hereinafter Wang) in view of Hamdi et al. (U.S. Pat. No. 6,912,651, hereinafter Hamdi). However, Applicants respectfully submit that these claims are patentable over Wang and Hamdi for the reasons provided below.

Independent Claim 1

Claim 1 recites "a first interface for direct connection to a memory bus which connects the host microprocessor and the system memory, such that the host controller is adapted to act only as a slave on the memory bus" (emphasis added).

In contrast, the combination of Wang and Hamdi does not teach a host controller with a direct connection to a memory bus so that the host controller acts only as a slave on the memory bus. The Office Action states that the proposed combination of references would have been obvious in order to reduce memory access latency because the USB host controller does not need to access the system memory through the microprocessor. While the Office Action attempts to address the limitations of the claim in isolation, the Office Action fails to appreciate that the proposed combination of Wang and Hamdi does not teach the limitations of the claim, as a whole. More specifically, the Office Action fails to appreciate that the system of Wang modified by the teachings of Hamdi cannot exhibit the functionality asserted in the Office Action. In order to

understand the implications of this reasoning, it may be useful to review the actual teachings of Wang and Hamdi.

Wang is directed to a USB host controller (the host controller system 100) which does not have bus mastering ability. Wang, paragraph 138, lines 1-4. Since the USB host controller of Wang does not have bus mastering ability, the USB host controller is connected to a host microprocessor, which controls the system bus between the host microprocessor and the system memory. Wang, Fig. 1A. The USB host controller accesses the system memory by data transfers through the host microprocessor. Wang, paragraph 35, lines 3-11. In order to execute USB transactions, the USB host controller sends interrupts to the host microprocessor for each USB transaction or for each batch of USB transactions. Wang, paragraph 38, line 6, through paragraph 39, line 15. While batching USB transactions and sending a single interrupt from the USB host controller to the host microprocessor may be more efficient than sending separate interrupts for each individual USB transaction, the USB host controller nevertheless always sends interrupts to the host microprocessor for one or more USB transactions. Thus, the USB host controller of Wang is only able to process USB transactions by interactions with the host microcontroller. Wang does not describe executing USB transactions, either individually or as a batch, without involvement from the host microprocessor.

Hamdi is generally directed to a system for providing a wireless USB bus between a computer and one or more peripheral USB devices so that the distances between the computer and the peripheral USB devices are not subject to the five meter limitation of USB cables. Hamdi, abstract. While Hamdi does not discuss USB host controllers in detail, Hamdi generally mentions that the computer includes a USB host controller to interface the USB bus to the host computer system. Hamdi, col. 1, lines 53-55. In a particular embodiment, the USB host controller connects to a microprocessor, within the host computer system, via a system bus. Hamdi, Fig. 6; col. 11, lines 47-48. Hamdi describes the USB host controller as operating to control and manage the USB bus. Hamdi, col. 11, lines 48-49; col. 6, lines 38-40 and 49-57; col. 9, lines 43-45; and col. 12, lines 40-41. However, Hamdi does not describe whether or not the USB host controller might control the system bus. In other words, Hamdi does not teach the USB host controller as operating to master the system bus. Conversely, Hamdi also fails to

teach the USB host controller as operating only as a slave on the system bus. Thus, Hamdi is silent as the ability, or lack of ability, of the USB host controller to potentially master the system bus.

With this overview of the teachings of Wang and Hamdi, it should be noted that Wang does not describe the USB host controller operating independently of the microcontroller. Nevertheless, the Office Action attempts to combine the teachings of Hamdi—directly connecting the USB host controller to the system bus—with the teachings Wang—the USB host controller accessing the system memory without mastering the bus—in order to purportedly allow the USB host controller to access the system memory without the involvement of the host microprocessor. More precisely, the Office Action asserts that the proposed combination would eliminate the need for the USB host controller to access the system memory through the host microprocessor. However, this reasoning is inaccurate because it fails to recognize that directly connecting, according to Hamdi, the USB host controller of Wang to the system bus of Wang does not change the functionality of the USB host controller of Wang to allow system memory access without the involvement of the microprocessor, as suggested in the Office Action. On the contrary, even if the USB host controller and system bus of Wang were directly connected, according to the configuration of Hamdi, the USB host controller would still operate according to the teachings of Wang by sending interrupts to the host microprocessor.

There is no description in either Wang or Hamdi of a USB host controller capable of accessing the system memory without the involvement of the host microprocessor. As explained above, Wang requires interrupts to the host microprocessor in order for the USB host controller to access the system memory. Additionally, it should be noted that Hamdi does not describe the USB host controller as operating to access system memory without involvement of the host microprocessor. While the USB host controller of Hamdi appears to be directly connected to the system bus, there is no description in Hamdi of whether or not the USB host controller might act as a master or a slave on the system bus. Thus, the proposed modification of Wang to change how the USB host controller might be connected to the host microprocessor does not change the fact that the USB host controller of Wang can only execute USB transactions by interrupting the host

microprocessor. Hence, the Office Action's reason for combining Wang and Hamdi, so that the USB host controller of Wang purportedly would not need the microcontroller to access the system memory, is inaccurate because the only way for the USB host controller of Wang to execute USB transactions is by interrupting the host microprocessor.

For the reasons presented above, the Office Action's reasoning presented in support of the obviousness rejection of the claim is insufficient because the Office Action's reasoning is inconsistent with the actual teachings of Wang and Hamdi. Also, the proposed combination of Wang and Hamdi does not teach all of the limitations of the claim because neither Wang nor Hamdi teaches a host controller which acts only as a slave on a memory bus. Accordingly, Applicants respectfully assert claim 1 is patentable over the combination of Wang and Hamdi because the combination of Wang and Hamdi does not teach all of the limitations of the claim.

Independent Claim 10

Applicants respectfully assert independent claim 10 is also patentable over the combination of Wang and Hamdi at least for similar reasons to those stated above in regard to the rejection of independent claim 1. In particular, claim 10 recites "a memory bus, which connects the host microprocessor and the system memory" and a host controller comprising "a first interface for direct connection to the memory bus, such that the host controller is adapted to act only as a slave on the memory bus" (emphasis added).

Here, although the language of claim 10 differs from the language of claim 1, and the scope of claim 10 should be interpreted independently of claim 1, Applicants respectfully assert that the remarks provided above in regard to the rejection of claim 1 also apply to the rejection of claim 10. Accordingly, Applicants respectfully assert claim 10 is patentable over the combination of Wang and Hamdi because the combination of Wang and Hamdi does not teach all of the limitations of the claim.

Dependent Claims

Claims 2-9 and 11-20 depend from and incorporate all of the limitations of the corresponding independent claims 1 and 10. Applicants respectfully assert claims 2-9 and 11-20 are allowable based on allowable base claims. Additionally, each of claims 2-9 and 11-20 may be allowable for further reasons.

CONCLUSION

Applicants respectfully request reconsideration of the claims in view of the remarks made herein. A notice of allowance is earnestly solicited.

Respectfully submitted,

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